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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,905	WILLINGHAM, SCOTT D.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8, 11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/29/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

4. Claims 1, 2, 13, 18, 20, 21, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 6,760,577 B2) in view of Healey et al. (US 4,434,407).

(1) Regarding claims 1, 18 and 22:

Li discloses a transceiver comprising:

an oscillator circuit (reference oscillator (Ref) and the first fractional phase-lock loop and the second fractional phase-lock loop in figure 3, column 5, lines 14-17 and 37-40) configured to generate a calibration tone (pilot tone, column 5, lines 37-40) and a phase locked loop (PLL) reference signal (first fractional phase-lock loop in figure 3, column 5, lines 14-17);

a phase locked loop circuit (first fractional phase-lock loop contains the main VOC in figure 3, column 5, lines 14-17) configured to generate a PLL output signal (output signal from the first fractional phase-lock loop) that is phase locked in relation to the PLL reference signal (column 5, lines 14-17);

a quadrature generator (device (90° / 0°) in figure 3) configured to generate quadrature mixer local oscillator (LO) signals derived from the PLL output signal (device (90° / 0°) in figure 3 take the output of the first fractional phase-lock loop and output a P1 and P2 signal to the mixers MR1 and MR2 respectively); and

an in-phase/quadrature (IQ) mixer configured to mix the calibration tone (pilot tone) with the quadrature mixer LO signals (the mixers MR1 and MR2 mixes with a quadrature local oscillator frequency, column 2, lines 17-28);

a first switch (SW1 in figure 3) coupled (through coupler C1) to selectively provide the calibration tone to the IQ mixer (Mr1 and MR2 in figure 3) during the calibration mode of operation (column 5, lines 38-40);

a reference signal to the phase locked loop circuit during the calibration mode of operation (reference oscillator (Ref) provides a reference signal to the phase locked loop when the pilot tone is being used, column 5, lines 14-17 and 37-40).

Li fails to disclose a second switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation.

However, Healey et al. discloses a switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit (an electronic switch S3 in figure 1 may be included to allow the frequency controller 52 to select between the crystal frequency generator 50 and the reference VCO frequency generator 56 to provide the reference frequency signal, column 3, lines 46-50).

It is desirable to have a switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation because it provides a reference signal for periodic calibration for achieving the stabilization (column 3, lines 51-56). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Healey et al. in the system of Li to improve the stability of the system.

(2) Regarding claim 2:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-8 and 11-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 16-17 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claims, or amend the claims to place the claims in proper dependent form, or rewrite the claim(s) in independent form. Claim 1 is the parent claim of claim 16. In the amendment dated 3/14/2007, the limitation "a second switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation" is being added to claim 1, claim 16 recites the same limitation.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

as applied to claims 1, 2, 13 and 18 above, and further in view of Wu et al. (US 6,968,167 B1).

(1) Regarding claim 3 and 19:

Li discloses a receiver circuit wherein during a calibration mode of operation, the oscillator is configured to operate near a particular frequency (pilot tone frequency, column 5, lines 37-40).

Li and Healey et al. fail to disclose the oscillator is operating in an open mode.

However, Wu et al. discloses a local oscillator generator (LO generator 14 in figure 2) that divides the reference signal and operates in an open loop mode (the reference frequency is from the crystal oscillator 38 and pass through a programmable divider DIVIDE/L 40 to generate the signal, column 9, lines 19-23).

It is desirable that during a calibration mode of operation the oscillator is configured to operate in an open loop mode because it requires less discrete components and be able to integrate into a single integrated circuit (column 1, lines 55-62). Therefore, it would have been obvious to replace the second phase-lock loop circuit of Li and Healey et al. that generate the pilot signal with the signal output from the DIVIDE/L 40 in Wu et al. for the pilot tone to reduce the size of the system.

(2) Regarding claim 4:

Li and Wu et al. disclose all of the subject matter as discussed in claim 3 but fail to explicitly discloses the reference oscillator (Ref in figure 3) is a voltage controlled oscillator.

However, Li discloses a main voltage controlled oscillator (main VCO in figure 3) in the first fractional phase-lock loop that can generate an oscillator signal.

It is well known in the art that a voltage controlled oscillator can generate an oscillator signal and be used to provide a reference oscillating signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to replace the reference signal oscillator (Ref in figure 3) with the main voltage controlled oscillator in the first fractional phase lock loop.

(3) Regarding claim 5:

Li further discloses a receiver circuit wherein the oscillator circuit includes a first divider circuit (in the first fractional phase-lock loop in figure 3, the ÷N1 block divide the Ref signal by N1 to generate the PLL reference signal) coupled to divide a frequency of the oscillator signal (reference frequency (Ref), column 5, lines 14-17) by a first amount (N1) to generate the PLL reference signal.

(4) Regarding claim 7:

Wu et al. further discloses a second divider circuit (programmable divider DIVIDE/L 40 in figure 2, column 9, lines 19-23) coupled to divide the frequency of the oscillator signal by a second amount (L) to generate the calibration tone.

(5) Regarding claim 8:

Wu further discloses the second divider circuit (programmable divider 40 in figure 2) is a programmable divider (divider 40 is programmable by the controller, column 8, line 7)

(6) Regarding claim 11:

Li discloses a receiver circuit wherein the oscillator circuit includes an oscillator configured to generate an oscillator signal (the main VCO in the first fractional phase-lock loop in figure 3 is configured to generate an oscillator signal, column 16-17).

(3) Regarding claim 13:

Li discloses a receiver wherein the IQ mixer (MR1 and MR2 in figure 3) generates an in-phase (I) signal (I_R in figure 3) and a quadrature (Q) signal (Q_R in figure 3) that are conveyed through an I channel and a Q channel, respectively, for processing by a baseband circuit ((column 1, lines 45-48).

(4) Regarding claim 20:

Li discloses a method further comprising dividing a frequency of an oscillator signal generated by the oscillator (in the first fractional phase-lock loop in figure 3, the ÷N1 block divide the Ref signal by N1 to generate the PLL reference signal) by a first amount (N1) to generate the PLL reference signal (output from the first fractional phase-lock loop).

(5) Regarding claim 21:

Li discloses a method further comprising dividing the frequency of the oscillator signal by a second amount to generate the calibration tone (pilot tone) (in the second fractional phase-lock loop in figure 3, the ÷N2 block divide the Ref signal by N2 to generate the PLL pilot tone by the second fractional phase-lock loop)

5. Claims 3, 4, 5, 7, 8, 11-12, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 6,760,577 B2) in view of Healey et al. (US 4,434,407)

Li discloses the receiver circuit wherein the first switch is further coupled to selectively (coupler C2 in figure 3) provide a receiver RF input signal to the IQ mixer (MT1 and MT2) during another mode of operation (column 5, lines 53-56).

(7) Regarding claim 12:

Li and Healey et al. fail to disclose the receiver circuit further comprising an amplifier coupled to amplify the receiver RF input signal prior to mixing in the IQ mixer.

However, Wu et al. discloses a receiver circuit further comprising an amplifier (amplifier LNA 22 in figure 2) coupled to amplify the receiver RF input signal prior to mixing in the IQ mixer (mixer 24 in figure 2, column 8, lines 20-24 and 31-33).

It is desirable to have the receiver circuit further comprising an amplifier coupled to amplify the receiver RF input signal prior to mixing in the IQ mixer because the amplifier provides high gain with good noise figure performance and can be integrated into a single chip transceiver (column 8, lines 20-22, column 11, lines 47-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Wu et al. with the system of Li and Healey et al. to improve the performance and reduce the size of the system.

(8) Regarding claim 16:

Claim 16 is rejected base on the reason as discuss in claim 1 in above.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 6,760,577 B2), Healey et al. (US 4,434,407) and Wu et al. (US 6,968,167 B1) as applied to claim 5 above, and further in view of Huscroft et al. (5,512,860).

Li, Healey et al. and Wu et al. disclose all the subject matter as discussed in claim 5 except fail to disclose wherein the first divider circuit is a power of two ripple divider.

However, Huscroft discloses a power of two ripple divider (ripple divider 29 in figure 2, column 6, lines 23-25).

It is desirable to use the power of two ripple divider for the first divider because it allows the use of a low cost ref oscillator to generate the reference signal (column 8, lines 39-42). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to replace the first divider of Li, Healey et al. and Wu by the ripple divider of Huscroft to reduce the production cost of the system.

7. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 6,760,577 B2) in view of Healey et al. (US 4,434,407) as applied to claim 13 above, and further in view of Liu (US 2003/0181187 A1).

(1) Regarding claim 14:

Li and Healey et al. disclose all the subject matter as discussed in claim 13 except the receiver circuit further comprising a calibration subsystem coupled to receive representations of the in-phase (I) signal and the quadrature (Q) signal, wherein the calibration subsystem is configured to determine one or more correction parameters for canceling a residual image signal.

However, Liu discloses an image-rejection I/Q demodulator to be used in a receiver that comprises a calibration subsystem (I/S detector 22 in figure 2 and a block

diagram of the Image/Signal Ratio it can enhance Detector in figure 3) coupled to receive representations of the in-phase (I) signal (I in figure 2) and the quadrature (Q) signal (Q in figure 2), wherein the calibration subsystem is configured to determine one or more correction parameters for canceling a residual image signal (amplitude control output 22c of the I/S detector and the phase control input 22d of the I/S detector in figure 3, paragraph 0033, lines 23-27).

It is desirable for the receiver circuit further comprising a calibration subsystem coupled to receive representations of the in-phase (I) signal and the quadrature (Q) signal, wherein the calibration subsystem is configured to determine one or more correction parameters for canceling a residual image signal because it enhances the image-rejection performance of digital communication receivers (paragraph 0017, lines 2-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Liu with the system of Li and Healey et al. to improve the performance of the receiver.

(2) Regarding claim 15:

Liu further discloses an analog-to-digital converter coupled to convert the I and Q signals generated by the IQ mixer to digital signals (A/D converter 211 and 212 in figure 3, paragraph 0033, lines 7-9).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 6,760,577 B2), Healey et al. (US 4,434,407) and Wu et al. (US 6,968,167 B1) as applied to claim 16 above, and further in view of Lee (US 2004/0086057 A1).

Li, Healey et al. and Wu et al. disclose all the subject matter as discuss in claim 16 except wherein during another mode of operation the oscillator is coupled to operate as a transmit oscillator within an offset phase locked loop circuit.

However, Lee et al. shows a communication transmitter with a oscillator (oscillator 26 in figure 4) coupled to operate as a transmit oscillator within an offset phase locked loop circuit (figure 4 discloses an offset phase locked loop transmitter that use an oscillator 26 operates as a transmit oscillator within an offset phase locked loop circuit 20 in figure 3 and 4, paragraph 0008-0010).

It is desirable to for the oscillator coupled to operate as a transmit oscillator within an offset phase locked loop circuit because it generates modulated signals in a more economical and power efficient manner (paragraph 0022). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Lee et al. with the system of Li, Healey et al. and Wu et al. to provide a more efficient system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M Lee
Examiner
Art Unit 2611
5/23/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER